DATA SHEET

TDA4858
Economy Autosync Deflection Controller (EASDC)

Preliminary specification
File under Integrated Circuits, IC02

1996 Jul 18

Philips Semiconductors

PHILIPS

Economy Autosync Deflection Controller (EASDC) TDA4858

FEATURES

Concept features

- Full Horizontal (H) plus Vertical (V) autosync capability
- Completely DC controllable for analog and digital concepts
- Excellent geometry control functions (e.g. automatic correction of East-West (EW) parabola during adjustment of vertical size and vertical shift)
- Flexible Switched Mode Power Supply (SMPS) function block for feedback and feed forward converters
- X-ray protection
- Start-up and switch-off sequence for safe operation of all power components
- Very good vertical linearity
- Internal supply voltage stabilization
- SDIP32 package.

Synchronization inputs

- Can handle all sync signals (Horizontal, Vertical, Composite and Sync-on-video)
- Combined output for video clamping, vertical blanking and protection blanking
- Start of video clamping pulses externally selectable.

Horizontal section

- Extremely low jitter
- Frequency locked loop for smooth catching of line frequency
- Simple frequency preset of f_{min} and f_{max} by external resistors
- DC controllable wide range linear picture position
- Soft start for horizontal driver.

Vertical section

- Vertical amplitude independent of frequency
- DC controllable picture height, picture position and S-correction
- Differential current outputs for DC coupling to vertical booster.

EW section

- Output for DC adjustable EW parabola
- DC controllable picture width and trapezium correction
- Optional tracking of EW parabola with line frequency
- Prepared for additional DC controls of vertical linearity, EW-corner, EW pin balance, EW parallelogram, vertical focus by extended application.

GENERAL DESCRIPTION

The TDA4858 is a high performance and efficient solution for autosync monitors. The concept is fully DC controllable and can be used in applications with a microcontroller and stand-alone in rock bottom solutions.

The TDA4858 provides synchronization processing, H + V synchronization with full autosync capability, and very short settling times after mode changes. External power components are given a great deal of protection. The IC generates the drive waveforms for DC-coupled vertical boosters such as TDA486X and TDA8351.

The TDA4858 provides extended functions e.g. as a flexible SMPS block and an extensive set of geometry control facilities, providing excellent picture quality.

Together with the Philips TDA488X video processor family a very advanced system solution is offered.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	9.2	–	16	V
I_{CC}	supply current	–	49	–	mA
ΔHPOS	horizontal shift adjustment range	–	±10.5	–	%
ΔVAMP	vertical size adjustment range	60	–	100	%
ΔVPOS	vertical shift adjustment range	–	±11.5	–	%
ΔVSCOR	vertical S-correction adjustment range	2	–	46	%
ΔV_{EWPAR}	EW parabola adjustment range	0.15	–	3.0	V
ΔV_{EWWID}	horizontal size adjustment range	0.2	–	4.0	V
ΔV_{EWTRP}	trapezium correction adjustment range	–	±0.5	–	V
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4858	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

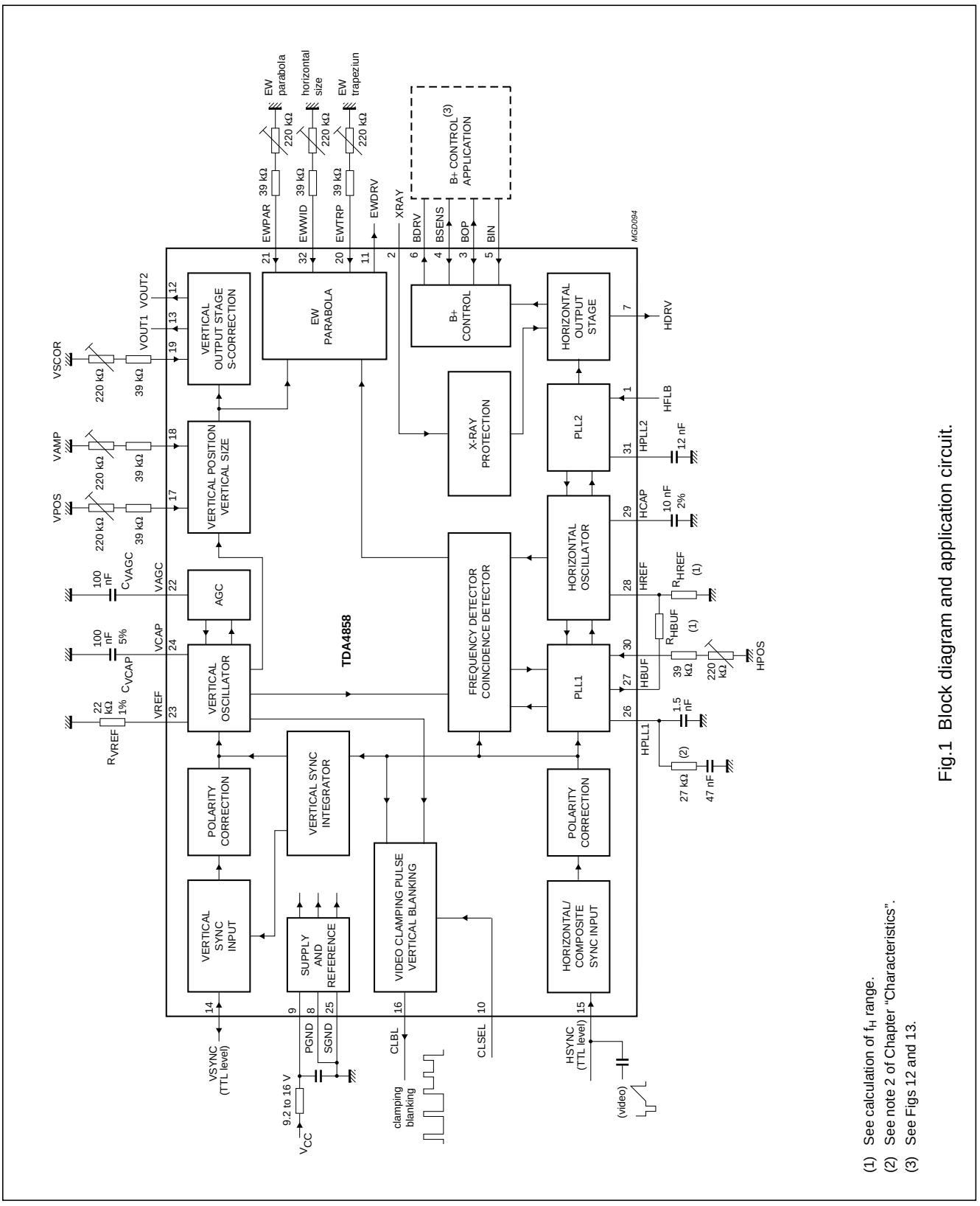


Fig.1 Block diagram and application circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output; comparator input
BSENS	4	B+ control comparator input/output
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
HDRV	7	horizontal driver output
PGND	8	power ground
V_{CC}	9	supply voltage
CLSEL	10	selection input for horizontal clamping trigger
EWDRV	11	EW parabola output
VOUT2	12	vertical output 2 (ascending sawtooth)
VOUT1	13	vertical output 1 (descending sawtooth)
VSYNC	14	vertical synchronization input/output (TTL level)
HSYNC	15	horizontal/composite synchronization input (TTL level or sync-on-video)
CLBL	16	video clamping pulse/vertical blanking and protection output
VPOS	17	vertical shift input
VAMP	18	vertical size input
VSCOR	19	vertical S-correction input
EWTRP	20	EW trapezium correction input
EWPAR	21	EW parabola amplitude input
VAGC	22	external capacitor for vertical amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
SGND	25	signal ground
HPLL1	26	external filter for PLL1
HBUF	27	buffered f/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HPOS	30	horizontal shift input
HPLL2	31	external filter for PLL2/soft start
EWWID	32	horizontal size input

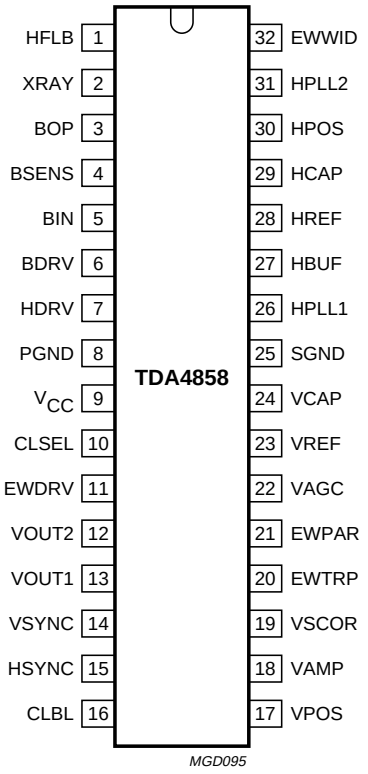


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

HSYNC (pin 15) is the input for horizontal synchronization signals, which can be DC-coupled TTL signals (horizontal or composite sync) and AC-coupled negative-going video sync signals. Video syncs are clamped to 1.28 V and sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to sync top.

For DC-coupled TTL signals the input clamping current is limited. The slicing level for TTL signals is 1.4 V.

The separated sync signal (either video or TTL) is integrated on an internal capacitor to detect and normalize the sync polarity.

Normalized horizontal sync pulses are used as input signals for the vertical sync integrator, the PLL1 phase detector and the frequency-locked loop.

Vertical sync integrator

Normalized composite sync signals from HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the horizontal oscillator reference current at HREF (pin 28). The integrator output directly triggers the vertical oscillator. This signal is available at VSYNC (normally vertical sync input; pin 14), which is used as an output in this mode.

Vertical sync slicer and polarity correction

Vertical sync signals (TTL) applied to VSYNC (pin 14) are sliced at 1.4 V. The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity.

If a composite sync signal is detected at HSYNC, VSYNC is used as output for the integrated vertical sync (e.g. for power saving applications).

Video clamping/vertical blanking generator

The video clamping/vertical blanking signal at CLBL (pin 16) is a two-level sandcastle pulse which is especially suitable for video ICs such as the TDA488X family, but also for direct applications in video output stages.

The upper level is the video clamping pulse, which is triggered by the trailing edge of the horizontal sync pulse. The width of the video clamping pulse is determined by an internal monoflop.

CLSEL (pin 10) is the selection input for the position of the video clamping pulse. If CLSEL is connected to ground, the clamping pulse is triggered with the trailing edge of horizontal sync. For a clamping pulse which starts with the leading edge of horizontal sync, pin 10 must be connected to V_{CC}.

The lower level of the sandcastle pulse is the vertical blanking pulse, which is derived directly from the internal oscillator waveform. It is started by the vertical sync and stopped with the start of the vertical scan. This results in optimum vertical blanking.

Blanking will be activated continuously, if one of the following conditions is true:

- No horizontal flyback pulses at HFLB (pin 1)
- X-ray protection is activated
- Soft start of horizontal drive (voltage at HPLL2 (pin 31) is low)
- Supply voltage at V_{CC} (pin 9) is low (see Fig.14)
- PLL1 is unlocked while frequency-locked loop is in search mode.

Blanking will not be activated if the horizontal sync frequency is below the valid range or there are no sync pulses available.

Frequency-locked loop

The frequency-locked loop can lock the horizontal oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and the recommended ratio is $\frac{f_{min}}{f_{max}} = \frac{1}{3.5}$

Larger ranges are possible by extended applications.

Without a horizontal sync signal the oscillator will be free-running at f_{min}. Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than 4% between horizontal sync and oscillator frequency switches the horizontal section into search mode. This means that PLL1 control currents are switched off immediately. Then the internal frequency detector starts tuning the oscillator. Very small DC currents at HPLL1 (pin 26) are used to perform this tuning with a well defined change rate. When coincidence between horizontal sync and oscillator frequency is detected, the search mode is replaced by a normal PLL operation. This operation ensures a smooth tuning and avoids fast changes of horizontal frequency during catching.

In this concept it is not allowed to load HPLL1.
The frequency dependent voltage at this pin is fed internally to HBUF (pin 27) via a sample-and-hold and buffer stage. The sample-and-hold stage removes all disturbances caused by horizontal sync or composite vertical sync from the buffered voltage. An external resistor from HBUF to HREF defines the frequency range.

See also hints for locking procedure in note 2 of Chapter “Characteristics”.

PLL1 phase detector

The phase detector is a standard type using switched current sources. It compares the middle of horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26).

Horizontal oscillator

The horizontal oscillator is of the relaxation type and requires a capacitor of 10 nF at HCAP (pin 29). For optimum jitter performance the value of 10 nF must not be changed.

The maximum oscillator frequency is determined by a resistor from HREF to ground. A resistor from HREF to HBUF defines the frequency range.

The reference current at HREF also defines the integration time constant of the vertical sync integration.

Calculation of line frequency range

First the oscillator frequencies f_{min} and f_{max} have to be calculated. This is achieved by adding the spread of the relevant components to the highest and lowest sync frequencies $f_{S(min)}$ and $f_{S(max)}$. The oscillator is driven by the difference of the currents in R_{HREF} and R_{HBUF}. At the highest oscillator frequency R_{HBUF} does not contribute to the spread. The spread will increase towards lower frequencies due to the contribution of R_{HBUF}. It is also dependent on the ratio $n_S = \frac{f_{S(max)}}{f_{S(min)}}$

The following example is a 31.45 to 64 kHz application:

$$n_S = \frac{f_{S(max)}}{f_{S(min)}} = \frac{64\ kHz}{31.45\ kHz} = 2.04$$

Table 1 Calculation of total spread

spread of:	for f_{max}	for f_{min}
IC	3%	3%
C_{HCAP}	2%	2%
R_{HREF}	1%	–
R_{HREF}, R_{HBUF}	–	$1\% \times (2.3 \times n_S - 1)$
Total	6%	8.69%

Thus the typical frequency range of the oscillator in this example is:

$$f_{max} = f_{S(max)} \times 1.06 = 67.84\ kHz$$

$$f_{min} = \frac{f_{S(min)}}{1.087} = 28.93\ kHz$$

The resistors R_{HREF} and R_{HBUF} can be calculated with the following formulae:

$$R_{HREF} = \frac{74 \times kHz \times k\Omega}{f_{max}\,[kHz]} = 1.091\ k\Omega$$

$$R_{HBUF} = \frac{R_{HREF} \times 1.19 \times n}{n-1} = 2.26\ k\Omega$$

Where: $n = \frac{f_{max}}{f_{min}} = 2.35$

The spread of f_{min} increases with the frequency ratio $\frac{f_{S(max)}}{f_{S(min)}}$.

For higher ratios this spread can be reduced by using resistors with less tolerances.

PLL2 phase detector

The PLL2 phase detector is similar to the PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of the HDRV (pin 7) output pulse.

The phase between horizontal flyback and horizontal sync can be controlled at HPOS (pin 30).

If HPLL2 is pulled to ground, horizontal output pulses, vertical output currents and B+ control driver pulses are inhibited. This means, HDRV (pin 7), BDRV (pin 6) VOUT1 (pin 13) and VOUT2 (pin 12) are floating in this state. PLL2 and the frequency-locked loop are disabled, and CLBL (pin 16) provides a continuous blanking signal.

This option can be used for soft start, protection and power-down modes. When the HPLL2 voltage is released again, an automatic soft start sequence will be performed (see Fig.15).

The soft start timing is determined by the filter capacitor at HPLL2 (pin 31), which is charged with an constant current during soft start. In the beginning the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty factor is reached. At this point BDRV (pin 6), VOUT1 (pin 13) and VOUT2 (pin 12) are re-enabled. The voltage at HPLL2 continues to rise until PLL2 enters its normal operating range. The internal charge current is now disabled. Finally PLL2 and the frequency-locked loop are enabled, and the continuous blanking at CLBL is removed.

Horizontal phase adjustment

HPOS (pin 30) provides a linear adjustment of the relative phase between the horizontal sync and oscillator sawtooth. Once adjusted, the relative phase remains constant over the whole frequency range.

Application hint: HPOS is a current input, which provides an internal reference voltage while I_{HPOS} is in the specified adjustment current range. By grounding HPOS the symmetrical control range is forced to its centre value, therefore the phase between horizontal sync and horizontal drive pulse is only determined by PLL2.

Output stage for line drive pulses

An open collector output stage allows direct drive of an inverting driver transistor because of a low saturation voltage of 0.3 V at 20 mA. To protect the line deflection transistor, the output stage is disabled (floating) for low supply voltage at V_{CC} (see Fig.14).

The duty factor of line drive pulses is slightly dependent on the actual line frequency. This ensures optimum drive conditions over the whole frequency range.

X-ray protection

The X-ray protection input XRAY (pin 2) provides a voltage detector with a precise threshold. If the input voltage at XRAY exceeds this threshold for a certain time, an internal latch switches the IC into protection mode. In this mode several pins are forced into defined states:

- Horizontal output stage (HDRV) is floating
- B+ control driver stage (BDRV) is floating
- Vertical output stages (VOUT1 and VOUT2) are floating
- CLBL provides a continuous blanking signal
- The capacitor connected to HPLL2 (pin 31) is discharged.

To reset the latch and return to normal operation, V_{CC} has to be temporarily switched off.

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of vertical amplitude after changes in sync frequency conditions. The free-running frequency $f_{osc(V)}$ is determined by the resistor R_{VREF} connected to pin 23 and the capacitor C_{VCAP} connected to pin 24. The value of R_{VREF} is not only optimized for noise and linearity performance in the whole vertical and EW section, but also influences several internal references. Therefore the value of R_{VREF} must not be changed. Capacitor C_{VCAP} should be used to select the free-running frequency of the vertical oscillator in accordance with the following formula:

$$f_{osc(V)} = \frac{1}{10.8 \times R_{VREF} \times C_{VCAP}}$$

To achieve a stabilized amplitude the free-running frequency $f_{osc(V)}$, without adjustment, should be at least 10% lower than the minimum trigger frequency.
The contributions shown in Table 2 can be assumed.

Table 2 Calculation of $f_{osc(V)}$ total spread

Contributing elements:	
Minimum frequency offset between $f_{osc(V)}$ and lowest trigger frequency	±10%
Spread of IC	±3%
Spread of R_{VREF}	±1%
Spread of C_{VCAP}	±5%
Total	19%

Result for 50 to 110 Hz application:

$$f_{osc(V)} = \frac{50\ Hz}{1.19} = 42\ Hz$$

Application hint: VAGC (pin 22) has a high input impedance during scan, thus the pin must not be loaded externally. Otherwise non-linearities in the vertical output currents may occur due to the changing charge current during scan.

Application hint: The full vertical sync range of 1 : 2.5 can be made usable by incorporating an adjustment of the free-running frequency. Also the complete sync range can be shifted to higher frequencies (e.g. 70 to 160 Hz) by reducing the value of C_{VCAP}.

Adjustment of vertical size, vertical shift and S-correction

VPOS (pin 17) is the input for the DC adjustable vertical picture shift. This pin provides a phase shift at the sawtooth output VOUT1 and VOUT2 (pins 13 and 12) and the EW drive output EWDRV (pin 11) in such a way, that the whole picture moves vertically while maintaining the correct geometry.

The amplitude of the differential output currents at VOUT1 and VOUT2 can be adjusted via input VAMP (pin 18). This can be a combination of a DC adjustment and a dynamic waveform modulation.

VSCOR (pin 19) is used to adjust the amount of vertical S-correction in the output signal.

The adjustments for vertical size and vertical shift also affect the waveforms of the EW parabola and the vertical S-correction. The result of this interaction is that no readjustment of these parameters is necessary after an adjustment of vertical picture size or position.

Application hint: VPOS is a current input, which provides an internal reference voltage while I_{VPOS} is in the specified adjustment current range. By grounding VPOS (pin 17) the symmetrical control range is forced to its centre value.

Application hint: VSCOR is a current input at 5 V. Superimposed on this level is a very small positive-going vertical sawtooth, intended to modulate an external long-tailed transistor pair. This enables further optional DC controls of functions which are not directly accessible such as vertical tilt or vertical linearity (see Fig.17).

EW parabola (including horizontal size and trapezium correction)

EWDRV (pin 11) provides a complete EW drive waveform. EW parabola amplitude, DC shift (horizontal size) and trapezium correction can be controlled via separate DC inputs.

EWPAR (pin 21) is used to adjust the parabola amplitude. This can be a combination of a DC adjustment and a dynamic waveform modulation.

The EW parabola amplitude also tracks with vertical picture size. The parabola waveform itself tracks with the adjustment for vertical picture shift (VPOS).

EWWID (pin 32) offers two modes of operation:

1. Mode 1

   Horizontal size is DC controlled via EWWID (pin 32) and causes a DC shift at the EWDRV output. Also the complete waveform is multiplied internally by a signal proportional to the line frequency (which is detected via the current at HREF (pin 28). This mode is to be used for driving EW modulator stages which require a voltage proportional to the line frequency.

2. Mode 2

   EWWID (pin 32) is grounded. Then EWDRV is no longer multiplied by the line frequency. The DC adjustment for horizontal size must be added to the input of the B+ control amplifier BIN (pin 5). This mode is to be used for driving EW modulators which require a voltage independent of the line frequency.

EWTRP (pin 20) is used to adjust the amount of trapezium correction in the EW drive waveform.

Application hint: EWTRP (pin 20) is a current input at 5 V. Superimposed on this level is a very small vertical parabola with positive tips, intended to modulate an external long-tailed transistor pair. This enables further optional DC controls of functions which are not directly accessible such as EW-corner, vertical focus or EW pin balance (see Fig.17).

Application hint: By grounding EWTRP (pin 20) the symmetrical control range is forced to its centre value.

B+ control function block

The B+ control function block of the EASDC consists of an Operational Transconductance Amplifier (OTA), a voltage comparator, a flip-flop and a discharge circuit.
This configuration allows easy applications for different B+ control concepts.

General description

The non-inverting input of the OTA is connected internally to a high precision reference voltage. The inverting input is connected to BIN (pin 5). An internal clamping circuit limits the maximum positive output voltage of the OTA.
The output itself is connected to BOP (pin 3) and to the inverting input of the voltage comparator.
The non-inverting input of the voltage comparator can be accessed via BSENS (pin 4).

B+ drive pulses are generated by an internal flip-flop and fed to BDRV (pin 6) via an open collector output stage. This flip-flop will be set at the rising edge of the signal at HDRV (pin 7). The falling edge of the output signal at BDRV has a defined delay of $t_{d(BDRV)}$ to the rising edge of the HDRV pulse. When the voltage at BSENS exceeds the voltage at BOP, the voltage comparator output resets the flip-flop, and therefore the open collector stage at BDRV is floating again.

An internal discharge circuit allows a well defined discharge of capacitors at BSENS. BDRV is active at a low level output voltage (see Figs 12 and 13), thus it requires an external inverting driver stage.

The B+ function block can be used for B+ deflection modulators in either of two modes:

- Feedback mode (see Fig.12)

  In this application the OTA is used as an error amplifier with a limited output voltage range. The flip-flop will be set at the rising edge of the signal at HDRV. A reset will be generated when the voltage at BSENS taken from the current sense resistor exceeds the voltage at BOP.

  If no reset is generated within a line period, the rising edge of the next HDRV pulse forces the flip-flop to reset. The flip-flop is set immediately after the voltage at BSENS has dropped below the threshold voltage $V_{RESTART(BSENS)}$.

- Feed forward mode (see Fig.13)

  This application uses an external RC combination at BSENS to provide a pulse width which is independent from the horizontal frequency. The capacitor is charged via an external resistor and discharged by the internal discharge circuit. For normal operation the discharge circuit is activated when the flip-flop is reset by the internal voltage comparator. Now the capacitor will be discharged with a constant current until the internally controlled stop level $V_{STOP(BSENS)}$ is reached. This level will be maintained until the rising edge of the next HDRV pulse sets the flip-flop again and disables the discharge circuit.

  If no reset is generated within a line period, the rising edge of the next HDRV pulse automatically starts the discharge sequence and resets the flip-flop (Fig.13). When the voltage at BSENS reaches the threshold voltage $V_{RESTART(BSENS)}$, the discharge circuit will be disabled automatically and the flip-flop will be set immediately. This behaviour allows a definition of the maximum duty cycle of the B+ control drive pulse by the relationship of charge current to discharge current.

Supply voltage stabilizer, references and protection

The ASDC provides an internal supply voltage stabilizer for excellent stabilization of all internal references. An internal gap reference especially designed for low-noise is the reference for the internal horizontal and vertical supply voltages. All internal reference currents and drive current for the vertical output stage are derived from this voltage via external resistors.

A special protection mode has been implemented in order to protect the deflection stages and the picture tube during start-up, shut-down and fault conditions. This protection mode can be activated as shown in Table 3.

Table 3 Activation of protection mode

ACTIVATION	RESET
Low supply voltage at pin 9	increase supply voltage
X-ray protection XRAY (pin 2) triggered	remove supply voltage
HPLL2 (pin 31) pulled to ground	release pin 31

When protection mode is active, several pins of the ASDC are forced into a defined state:

HDRV (horizontal driver output) is floating

BDRV (B+ control driver output) is floating

VOUT1 and VOUT2 (vertical outputs) are floating

CLBL provides a continuous blanking signal

The capacitor at HPLL2 is discharged.

If the protection mode is activated via the supply voltage at pin 9, all these actions will be performed in a well defined sequence (see Fig.14). For activation via X-ray protection or HPLL2 all actions will occur simultaneously.

The return to normal operation is performed in accordance with the start-up sequence in Fig.14a, if the reset was caused by the supply voltage at pin 9. The first action with increasing supply voltage is the activation of continuous blanking at CLBL. When the threshold for activation of HDRV is passed, an internal current begins to charge the external capacitor at HPLL2 and a PLL2 soft start sequence is performed (see Fig.15). In the beginning of this phase the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty cycle is reached. Then the PLL2 voltage passes the threshold for activation of BDRV, VOUT1 and VOUT2.

For activation of these pins not only the PLL2 voltage, but also the supply voltage must have passed the appropriate threshold. A last pair of thresholds has to be passed by PLL2 voltage **and** supply voltage before the continuous blanking is finally removed, and the operation of PLL2 and frequency-locked loop is enabled.

A return to the normal operation by releasing the voltage at HPLL2 will lead to a slightly different sequence. Here the activation of all functions is influenced only by the voltage at HPLL2 (see Fig.15).

Application hint: Internal discharge of the capacitor at HPLL2 will only be performed, if the protection mode was activated via the supply voltage or X-ray protection.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all voltages measured with respect to ground.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+16	V
$V_{I(n)}$	input voltages			
	BIN	–0.5	+6.0	V
	HSYNC, VPOS, VAMP, VSCOR, VREF, HREF and HPOS	–0.5	+6.5	V
	XRAY	–0.5	+8.0	V
	CLSEL	–0.5	+16	V
$V_{O(n)}$	output voltages			
	VOUT1 and VOUT2	–0.5	+6.5	V
	BDRV and HDRV	–0.5	+16	V
$V_{I/O(n)}$	input/output voltages			
	BOP and BSENS	–0.5	+6.0	V
	VSYNC	–0.5	+6.5	V
I_{HDRV}	horizontal driver output current	–	100	mA
I_{HFLB}	horizontal flyback input current	–10	+10	mA
I_{CLBL}	video clamping pulse/vertical blanking output current	–	–10	mA
I_{BOP}	B+ control OTA output current	–	1	mA
I_{BDRV}	B+ control driver output current	–	50	mA
I_{EWDRV}	EW driver output current	–	–5	mA
T_{amb}	operating ambient temperature	0	70	°C
T_j	junction temperature	–	150	°C
T_{stg}	storage temperature	–55	+150	°C
V_{esd}	electrostatic discharge for all pins (note 1)			
	machine model	–400	+400	V
	human body model	–3000	+3000	V

Note

1. Machine model: 200 pF, 25 Ω, 2.5 μH; human body model: 100 pF, 1500 Ω, 7.5 μH.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W

QUALITY SPECIFICATION

In accordance with *"URF-4-2-59/601"*; EMC emission/immunity test in accordance with *"DIS 1000 4.6"* (IEC 801.6)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EMC}	emission test	note 1	–	1.5	–	mV
	immunity test	note 1	–	2.0	–	V

Note

1. Tests are performed with application reference board. Tests with other boards will have different results.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; peripheral components in accordance with Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal sync separator						
INPUT CHARACTERISTICS FOR DC-COUPLED TTL SIGNALS [HSYNC (PIN 15)]						
$V_{DC(HSYNC)}$	sync input signal voltage		1.7	–	–	V
	slicing voltage level		1.2	1.4	1.6	V
$t_{r(HSYNC)}$	rise time of sync pulse		10	–	500	ns
$t_{f(HSYNC)}$	fall time of sync pulse		10	–	500	ns
$t_{W(HSYNC)}$	minimum width of sync pulse		0.7	–	–	µs
$I_{DC(HSYNC)}$	input current	V_{HSYNC} = 0.8 V	–	–	–200	µA
		V_{HSYNC} = 5.5 V	–	–	10	µA
INPUT CHARACTERISTICS FOR AC-COUPLED VIDEO SIGNALS (SYNC-ON-VIDEO, NEGATIVE SYNC POLARITY)						
$V_{AC(HSYNC)}$	sync amplitude of video input signal voltage		–	300	–	mV
	slicing voltage level (measured from top sync)	source resistance R_S = 50 Ω	90	120	150	mV
$V_{clamp(HSYNC)}$	top sync clamping voltage level		1.1	1.28	1.5	V
$I_{C(HSYNC)}$	charge current for coupling capacitor	$V_{HSYNC} > V_{clamp(HSYNC)}$	1.7	2.4	3.4	µA
$t_{HSYNC(min)}$	minimum width of sync pulse		0.7	–	–	µs
$R_{S(max)}$	maximum source resistance	duty factor = 7%	–	–	1500	Ω
$r_{diff(HSYNC)}$	differential input resistance	during sync	–	80	–	Ω
Automatic polarity correction for horizontal sync						
$\frac{t_{P(H)}}{t_H}$	horizontal sync pulse width related to t_H	f_H < 45 kHz	–	–	20	%
		f_H > 45 kHz	–	–	25	%
$t_{P(H)}$	delay time for changing polarity		0.3	–	1.8	ms
Vertical sync integrator						
$t_{int(V)}$	integration time for generation of a vertical trigger pulse	f_H = 31.45 kHz; I_{HREF} = 1.052 mA	7	10	13	µs
		f_H = 64 kHz; I_{HREF} = 2.141 mA	3.9	5.7	6.5	µs
		f_H = 100 kHz; I_{HREF} = 3.345 mA	2.5	3.8	4.5	µs
Vertical sync slicer (DC-coupled, TTL compatible) [VSYNC (pin 14)]						
V_{VSYNC}	sync input signal voltage		1.7	–	–	V
	slicing voltage level		1.2	1.4	1.6	V
I_{VSYNC}	input current	0 V < V_{SYNC} < 5.5 V	–	–	±10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VERTICAL SYNC OUTPUT AT VSYNC (PIN 14) DURING COMPOSITE SYNC AT HSYNC (PIN 15)						
I_{VSYNC}	output current	during internal vertical sync	–0.7	–1.0	–1.35	mA
V_{VSYNC}	internal clamping voltage level	during internal vertical sync	4.4	4.8	5.2	V
	steepness of slopes		–	300	–	ns/mA
Automatic polarity correction for vertical sync						
$t_{VSYNC(max)}$	maximum width of vertical sync pulse		–	–	300	µs
$t_{d(VPOL)}$	delay for changing polarity		0.3	–	1.8	ms
Video clamping/vertical blanking output [CLBL (pin 16)]						
$t_{clamp(CLBL)}$	width of video clamping pulse	measured at V_{CLBL} = 3 V	0.6	0.7	0.8	µs
$V_{clamp(CLBL)}$	top voltage level of video clamping pulse		4.32	4.75	5.23	V
TC_{clamp}	temperature coefficient of $V_{clamp(CLBL)}$		–	+4	–	mV/K
	steepness of slopes for clamping pulse	R_L = 1 MΩ; C_L = 20 pF	–	50	–	ns/V
$V_{blank(CLBL)}$	top voltage level of vertical blanking pulse	note 1	1.7	1.9	2.1	V
$t_{blank(CLBL)}$	width of vertical blanking pulse		240	300	360	µs
TC_{blank}	temperature coefficient of $V_{blank(CLBL)}$		–	+2	–	mV/K
$V_{scan(CLBL)}$	output voltage during vertical scan	I_{CLBL} = 0	0.59	0.63	0.67	V
TC_{scan}	temperature coefficient of $V_{scan(CLBL)}$		–	–2	–	mV/K
$I_{sink(CLBL)}$	internal sink current		2.4	–	–	mA
$I_{load(CLBL)}$	external load current		–	–	–3.0	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SELECTION OF LEADING/TRAILING EDGE TRIGGER FOR VIDEO CLAMPING PULSE						
V_{CLSEL}	voltage at CLSEL (pin 10) for trigger with leading edge of horizontal sync		7	–	V_{CC}	V
	voltage at CLSEL for trigger with trailing edge of horizontal sync		0	–	5	V
$t_{d(clamp)}$	delay between leading edge of horizontal sync and start of horizontal clamping pulse	V_{CLSEL} > 7 V	–	300	–	ns
	delay between trailing edge of horizontal sync and start of horizontal clamping pulse	V_{CLSEL} < 5 V	–	130	–	ns
$t_{clamp(max)}$	maximum duration of video clamping pulse after end of horizontal sync	V_{CLBL} = 3 V; V_{CLSEL} > 7 V	–	–	0.15	µs
		V_{CLBL} = 3 V; V_{CLSEL} < 5 V	–	–	1.0	µs
R_{CLSEL}	input resistance at CLSEL (pin 10)	$V_{CLSEL} \leq V_{CC}$	80	–	–	kΩ
PLL1 phase comparator and frequency-locked loop [HPLL1 (pin 26) and HBUF (pin 27)]						
$t_{HSYNC(max)}$	maximum width of horizontal sync pulse (referenced to line period)	f_H < 45 kHz; note 2	–	–	20	%
		f_H > 45 kHz; note 2	–	–	25	%
$t_{lock(HPLL1)}$	total lock-in time of PLL1		–	40	80	ms
V_{HPLL1}	control voltage	notes 3 and 4				
V_{HBUF}	buffered f/v voltage at HBUF (pin 27)	$f_{H(min)}$; note 5	–	5.6	–	V
		$f_{H(max)}$; note 5	–	2.5	–	V
$I_{load(HBUF)}$	maximum load current		–	–	–4.0	mA
ADJUSTMENT OF HORIZONTAL PICTURE POSITION						
ΔHPOS	horizontal shift adjustment range (referenced to horizontal period)	I_{HSHIFT} = 0	–	–10.5	–	%
		I_{HSHIFT} = –135 µA	–	+10.5	–	%
I_{HPOS}	input current	ΔHPOS = +10.5%	–110	–120	–135	µA
		ΔHPOS = –10.5%	–	0	–	µA
$V_{ref(HPOS)}$	reference voltage at input	note 6	–	5.1	–	V
$V_{off(HPOS)}$	picture shift is centred if HPOS (pin 30) is forced to ground		0	–	0.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal oscillator [HCAP (pin 29) and HREF (pin 28)]						
$f_{H(0)}$	free-running frequency without PLL1 action (for testing only)	$R_{HBUF} = \infty$; R_{HREF} = 2.4 kΩ; C_{HCAP} = 10 nF; note 4	30.53	31.45	32.39	kHz
$\Delta f_{H(0)}$	spread of free-running frequency (excluding spread of external components)		–	–	±3.0	%
TC	temperature coefficient of free-running frequency		–100	0	+100	10^{-6}/K
$f_{H(max)}$	maximum oscillator frequency		–	–	130	kHz
V_{HREF}	voltage at input for reference current		2.43	2.55	2.68	V
PLL2 phase detector [HFLB (pin 1) and HPLL2 (pin 31)]						
$\Delta\phi_{PLL2}$	PLL2 control (advance of horizontal drive with respect to middle of horizontal flyback)	maximum advance	36	–	–	%
		minimum advance	–	7	–	%
$t_{d(HFLB)}$	delay between middle of horizontal sync and middle of horizontal flyback	HPOS (pin 30) grounded	–	200	–	ns
$V_{PROT(HPLL2)}$	maximum voltage for PLL2 protection mode/soft start		–	4.4	–	V
$I_{charge(HPLL2)}$	charge current for external capacitor during soft start	V_{HPLL2} < 3.7 V	–	15	–	µA
HORIZONTAL FLYBACK INPUT [HFLB (PIN 1)]						
V_{HFLB}	positive clamping level	I_{HFLB} = 5 mA	–	5.5	–	V
	negative clamping level	I_{HFLB} = –1 mA	–	–0.75	–	V
I_{HFLB}	positive clamping current		–	–	6	mA
	negative clamping current		–	–	–2	mA
V_{HFLB}	slicing level		–	2.8	–	V
Output stage for line driver pulses [HDRV (pin 7)]						
OPEN COLLECTOR OUTPUT STAGE						
V_{HDRV}	saturation voltage	I_{HDRV} = 20 mA	–	–	0.3	V
		I_{HDRV} = 60 mA	–	–	0.8	V
$I_{leakage(HDRV)}$	output leakage current	V_{HDRV} = 16 V	–	–	10	µA
AUTOMATIC VARIATION OF DUTY FACTOR						
$t_{HDRV(OFF)}/t_H$	relative t_{OFF} time of HDRV output; measured at V_{HDRV} = 3 V; HDRV duty factor is determined by the relation I_{HREF}/I_{VREF}	I_{HDRV} = 20 mA; f_H = 31.45 kHz; see Fig.9	42	45	48	%
		I_{HDRV} = 20 mA; f_H = 57 kHz; see Fig.9	45	46.3	47.7	%
		I_{HDRV} = 20 mA; f_H = 90 kHz; see Fig.9	46.6	48	49.4	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
X-ray protection [XRAY (pin 2)]						
V_{XRAY}	slicing voltage level		6.14	6.38	6.64	V
$t_{W(XRAY)}$	minimum width of trigger pulse		10	–	–	µs
$R_{I(XRAY)}$	input resistance at XRAY (pin 2)	$V_{XRAY} < 6.38\ V + V_{BE}$	500	–	–	kΩ
		$V_{XRAY} > 6.38\ V + V_{BE}$	–	5	–	kΩ
$V_{RESET(VCC)}$	supply voltage for reset of X-ray latch		–	5.6	–	V
Vertical oscillator (oscillator frequency in application without adjustment of free-running frequency $f_{v(o)}$)						
f_V	free-running frequency	R_{VREF} = 22 kΩ; C_{VCAP} = 100 nF	40	42	43.3	Hz
$f_{v(o)}$	vertical frequency catching range	constant amplitude; notes 7, 8 and 9	50	–	110	Hz
V_{VREF}	voltage at reference input for vertical oscillator		–	3.0	–	V
$t_{d(scan)}$	delay between trigger pulse and start of ramp at VCAP (pin 24) (width of vertical blanking pulse)		240	300	360	µs
I_{VAGC}	control currents of amplitude control		±120	±200	±300	µA
C_{VAGC}	external capacitor at VAGC (pin 22)		–	–	150	nF
Differential vertical current outputs						
ADJUSTMENT OF VERTICAL SIZE (see Figs 3 to 8) [VAMP (PIN 18)]						
ΔVAMP	vertical size adjustment range (referenced to nominal vertical size)	I_{VAMP} = 0; note 10	–	60	–	%
		I_{VAMP} = –135 µA; note 10	–	100	–	%
I_{VAMP}	input current for maximum amplitude (100%)		–110	–120	–135	µA
	input current for minimum amplitude (60%)		–	0	–	µA
$V_{ref(VAMP)}$	reference voltage at input		–	5.0	–	V
ADJUSTMENT OF VERTICAL SHIFT (see Figs 3 to 8) [VPOS (PIN 17)]						
ΔVPOS	vertical shift adjustment range (referenced to 100% vertical size)	I_{VPOS} = –135 µA; note 10	–	–11.5	–	%
		I_{VPOS} = 0; note 10	–	+11.5	–	%
I_{VPOS}	input current for maximum shift-up		–110	–120	–135	µA
	input current for maximum shift-down		–	0	–	µA
$V_{ref(VPOS)}$	reference voltage at input		–	5.0	–	V
$V_{off(VPOS)}$	vertical shift is centred if VPOS (pin 17) is forced to ground		0	–	0.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADJUSTMENT OF VERTICAL S-CORRECTION (see Figs 3 to 8) [VSCOR (PIN 19)]						
ΔVSCOR	vertical S-correction adjustment range	I_{VSCOR} = 0; note 10	–	2	–	%
		I_{VSCOR} = –135 µA; note 10	–	46	–	%
I_{VSCOR}	input current for maximum S-correction		–110	–120	–135	µA
	input current for minimum S-correction		–	0	–	µA
δVSCOR	symmetry error of S-correction	maximum ΔVSCOR	–	–	±0.7	%
$V_{ref(VSCOR)}$	reference voltage at input		–	5.0	–	V
$V_{SAWM(p-p)}$	voltage amplitude of superimposed logarithmic sawtooth (peak-to-peak value)	note 11	–	–	145	mV
Vertical output stage [VOUT1 (pin 13) and VOUT2 (pin 12)]						
$\Delta I_{VOUT(nom)}$	nominal differential output current (peak-to-peak value) ($\lvert\Delta I_{VOUT}\rvert = I_{VOUT1} - I_{VOUT2}$)	nominal settings; note 10	0.76	0.85	0.94	mA
$\Delta I_{VOUT(max)}$	maximum differential output current (peak value) ($\lvert\Delta I_{VOUT}\rvert = I_{VOUT1} - I_{VOUT2}$)		0.47	0.52	0.57	mA
V_{VOUT1}, V_{VOUT2}	allowed voltage at outputs		0	–	4.2	V
$\delta_{V(offset)}$	maximum offset error of vertical output currents	nominal settings; note 10	–	–	±2.5	%
$\delta_{V(lin)}$	maximum linearity error of vertical output currents	nominal settings; note 10	–	–	±1.5	%
EW drive output						
EW DRIVE OUTPUT STAGE [EWDRV (PIN 11)]						
V_{EWDRV}	bottom output voltage (internally stabilized)	$V_{PAR(EWDRV)}$ = 0; $V_{DC(EWDRV)}$ = 0; EWTRP centred	1.05	1.2	1.35	V
	maximum output voltage	note 12	7.0	–	–	V
I_{EWDRV}	output load current		–	–	±2.0	mA
TC_{EWDRV}	temperature coefficient of output signal		–	–	600	10^{-6}/K
ADJUSTMENT OF EW PARABOLA AMPLITUDE (see Figs 3 to 8) [EWPAR (PIN 21)]						
$V_{PAR(EWDRV)}$	parabola amplitude	I_{EWPAR} = 0; note 10	–	0.05	–	V
		I_{EWPAR} = –135 µA; note 10	–	3	–	V
I_{EWPAR}	input current for maximum amplitude		–110	–120	–135	µA
	input current for minimum amplitude		–	0	–	µA
$V_{ref(EWPAR)}$	reference voltage at input		–	5.0	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADJUSTMENT OF HORIZONTAL SIZE (see Figs 3 to 8) [EWWID (PIN 32)]						
$V_{DC(EWDRV)}$	EW parabola DC voltage shift	I_{EWWID} = −135 μA; note 10	–	0.1	–	V
		I_{EWWID} = 0; note 10	–	4.2	–	V
I_{EWWID}	input current for maximum DC shift		–	0	–	μA
	input current for minimum DC shift		−110	−120	−135	μA
$V_{ref(EWWID)}$	reference voltage at input		–	5.0	–	V
ADJUSTMENT OF TRAPEZIUM CORRECTION (see Figs 3 to 8) [EWTRP (PIN 20)]						
$V_{TRP(EWTRP)}$	trapezium correction voltage	I_{EWTRP} = 0; note 10	–	−0.5	–	V
		I_{EWTRP} = −135 μA; note 10	–	+0.5	–	V
I_{EWTRP}	input current for maximum positive trapezium correction		−110	−120	−135	μA
	input current for maximum negative trapezium correction		–	0	–	μA
$V_{ref(EWTRP)}$	reference voltage at input		–	5.0	–	V
$V_{off(EWTRP)}$	trapezium correction is centred if EWTRP (pin 20) is forced to ground		0	–	0.1	V
$V_{PARM(p-p)}$	amplitude of superimposed logarithmic parabola (peak-to-peak value)	note 13	–	–	145	mV
TRACKING OF EWDRV OUTPUT SIGNAL WITH f_H PROPORTIONAL VOLTAGE						
$f_{H(MULTI)}$	f_H range for tracking		24	–	80	kHz
$V_{PAR(EWDRV)}$	parabola amplitude at EWDRV (pin 11)	I_{HREF} = 1.052 mA; f_H = 31.45 kHz; note 14	1.3	1.45	1.6	V
		I_{HREF} = 2.341 mA; f_H = 70 kHz; note 14	2.7	3.0	3.3	V
		function disabled; note 14	2.7	3.0	3.3	V
δV_{EWDRV}	linearity error of f_H tracking		–	–	8	%
V_{EWWID}	voltage range to inhibit tracking		0	–	0.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B+ control section (see Figs 12 and 13)						
TRANSCONDUCTANCE AMPLIFIER [BIN (PIN 5) AND BOP (PIN 3)]						
V_{BIN}	input voltage		0	–	5.25	V
$I_{BIN(max)}$	maximum input current		–	–	±1	µA
$V_{ref(int)}$	reference voltage at internal non-inverting input of OTA		2.37	2.5	2.58	V
$V_{BOP(min)}$	minimum output voltage		–	0.4	–	V
$V_{BOP(max)}$	maximum output voltage	I_{BOP} < 1 mA	5.0	5.3	5.6	V
$I_{BOP(max)}$	maximum output current		–	±500	–	µA
g	transconductance of OTA	note 15	30	50	70	mS
G_{open}	open-loop gain	note 16	–	86	–	dB
C_{BOP}	minimum value of capacitor at BOP (pin 3)		4.7	–	–	nF
VOLTAGE COMPARATOR [BSENS (PIN 4)]						
V_{BSENS}	voltage range of positive comparator input		0	–	5	V
V_{BOP}	voltage range of negative comparator input		0	–	5	V
I_{BSENS}	maximum leakage current	discharge disabled	–	–	–2	µA
OPEN COLLECTOR OUTPUT STAGE [BDRV (PIN 6)]						
$I_{BDRV(max)}$	maximum output current		20	–	–	mA
$I_{leakage(BDRV)}$	output leakage current	V_{BDRV} = 16 V	–	–	3	µA
$V_{sat(BDRV)}$	saturation voltage	I_{BDRV} < 20 mA	–	–	300	mV
$t_{off(min)}$	minimum off-time		–	250	–	ns
$t_{d(BDRV)}$	delay between BDRV pulse and HDRV pulse (rising edges)	measured at V_{HDRV}, V_{BDRV} = 3 V	–	500	–	ns
BSENS DISCHARGE CIRCUIT						
$V_{STOP(BSENS)}$	discharge stop level	capacitive load; I_{BSENS} = 0.5 mA	0.85	1.0	1.15	V
$I_{DISC(BSENS)}$	discharge current	V_{BSENS} > 2.5 V	4.5	6.0	7.5	mA
$V_{RESTART(BSENS)}$	threshold voltage for restart	fault condition	1.2	1.3	1.4	V
C_{BSENS}	minimum value of capacitor at BSENS (pin 4)		2	–	–	nF
Internal reference, supply voltage and protection						
$V_{STAB(VCC)}$	external supply voltage for complete stabilization of all internal references		9.2	–	16	V
I_{VCC}	supply current		–	49	–	mA
PSRR	power supply rejection ratio of internal supply voltage	f = 1 kHz	50	–	–	dB

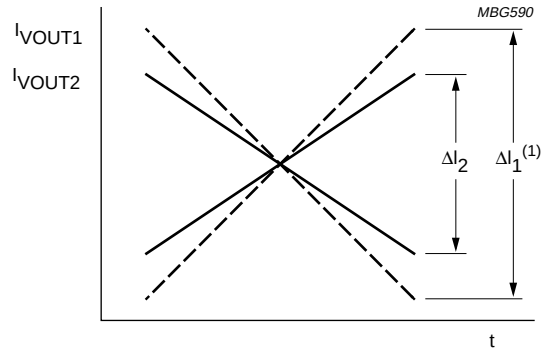
Notes to the characteristics

1. Continuous blanking at CLBL (pin 16) will be activated, if one of the following conditions is true:
   a) No horizontal flyback pulses at HFLB (pin 1) within a line
   b) X-ray protection is triggered
   c) Voltage at HPLL2 (pin 31) is low (for soft start of horizontal drive)
   d) Supply voltage at V_{CC} (pin 9) is low
   e) PLL1 unlocked while frequency-locked loop is in search mode.
2. To ensure safe locking of the horizontal oscillator, one of the following procedures is required:
   a) Search mode starts always from f_{min}. Then the PLL1 filter components are a 3.3 nF capacitor from pin 26 to ground in parallel with an 8.2 kΩ resistor in series with a 47 nF capacitor.
   b) Search mode starts either from f_{min} or f_{max} with HPOS in middle position (I_{HPOS} = 60 μA). Then the PLL1 filter components are a 1.5 nF capacitor from pin 26 to ground in parallel with a 27 kΩ resistor in series with a 47 nF capacitor.
   c) After locking is achieved, HPOS can be operated in the normal way.
3. Loading of HPLL1 (pin 26) is not allowed.
4. Oscillator frequency is f_{min} when no sync input signal is present (no continuous blanking at pin 16).
5. Voltage at HPLL1 (pin 26) is fed to HBUF (pin 27) via a buffer. Disturbances caused by horizontal sync are removed by an internal sample-and-hold circuit.
6. Input resistance at HPOS (pin 30): $R_{HPOS} = \frac{kT}{q} \times \frac{1}{I_{HPOS}}$
7. Full vertical sync range with constant amplitude ($f_{V(min)} : f_{V(max)}$ = 1 : 2.5) can be made usable by choosing an application with adjustment of free-running frequency.
8. If higher vertical frequencies are required, sync range can be shifted by using a smaller capacitor at VCAP (pin 24).
9. Value of resistor at VREF (pin 23) may not be changed.
10. All vertical and EW adjustments are specified at nominal vertical settings, which means:
    a) ΔVAMP = 100% (I_{VAMP} = 135 μA)
    b) ΔVSCOR = 0 (pin 19 open-circuit)
    c) ΔVPOS centred (pin 17 forced to ground)
    d) f_H = 70 kHz.
11. The superimposed logarithmic sawtooth at VSCOR (pin 19) tracks with VPOS, but **not** with VAMP settings.

    The superimposed waveform is described by $\frac{kT}{q} \times \ln\frac{1-d}{1+d}$ with 'd' being the modulation depth of a sawtooth from $-\frac{5}{6}$ to $+\frac{5}{6}$. A linear sawtooth with the same modulation depth can be recovered in an external long-tailed pair (see Fig.17).
12. The output signal at EWDRV (pin 11) may consist of parabola + DC shift + trapezium correction. These adjustments have to be carried out in a correct relationship to each other in order to avoid clipping due to the limited output voltage range at EWDRV.
13. The superimposed logarithmic parabola at EWTRP (pin 20) tracks with VPOS, but **not** with VAMP settings (see Fig.17).
14. If f_H tracking is enabled, the amplitude of the complete EWDRV output signal (parabola + DC shift + trapezium) will be changed proportional to I_{HREF}. The EWDRV low level of 1.2 V remains fixed.
15. First pole of transconductance amplifier is 5 MHz without external capacitor (will become the second pole, if the OTA operates as an integrator).

16. Open-loop gain is $\frac{V_{BOP}}{V_{BIN}}$ at f = 0 with no resistive load and C_{BOP} = 4.7 nF (from BOP (pin 3) to GND).

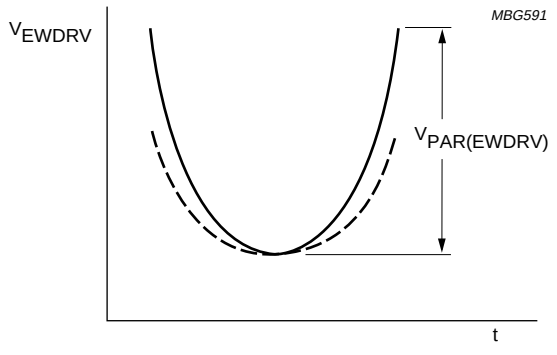
Vertical and EW adjustments



(1) ΔI_1 is the maximum amplitude setting at VAMP (pin 18); VPOS centred and VSCOR = 0%.

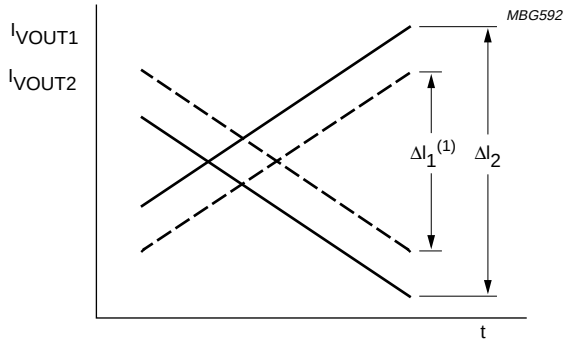
$\Delta VAMP = \frac{\Delta I_2}{\Delta I_1} \times 100\%$

Fig.3 I_{VOUT1} and I_{VOUT2} as functions of time.



$\Delta EWPAR$ = 0 to $V_{PAR(EWDRV)}$.

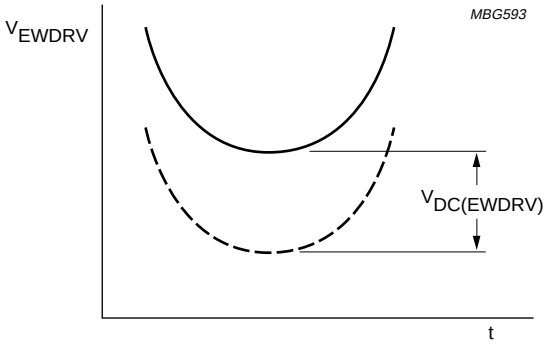
Fig.4 V_{EWDRV} as a function of time.



(1) ΔI_1 is VPOS adjustment centred; maximum amplitude setting at VAMP (pin 18).

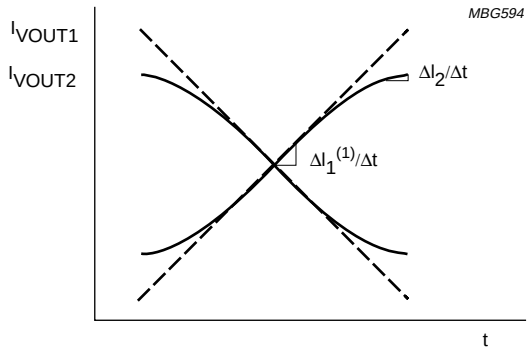
$$\Delta VPOS = \frac{\Delta I_2 - \Delta I_1}{2 \times \Delta I_1} \times 100\%$$

Fig.5 I_{VOUT1} and I_{VOUT2} as functions of time.



$\Delta EWWID$ = 0 to $V_{DC(EWDRV)}$.

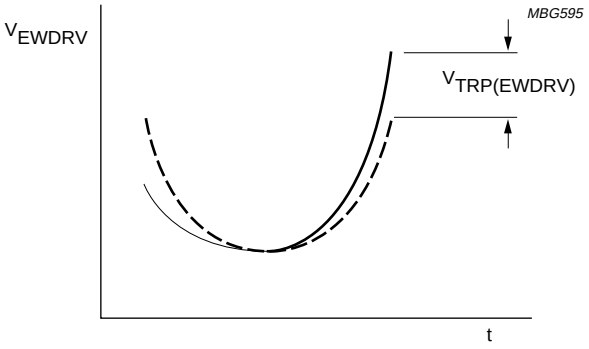
Fig.6 V_{EWDRV} as a function of time.



(1) ΔI_1 is VSCOR = 0%; maximum amplitude setting at VAMP (pin 18).

$$\Delta VSCOR = \frac{\Delta I_1 - \Delta I_2}{\Delta I_1} \times 100\%$$

Fig.7 I_{VOUT1} and I_{VOUT2} as functions of time.



$\Delta EWTRP = \pm V_{TRP(EWDRV)}$.

Fig.8 V_{EWDRV} as a function of time.

Pulse diagrams

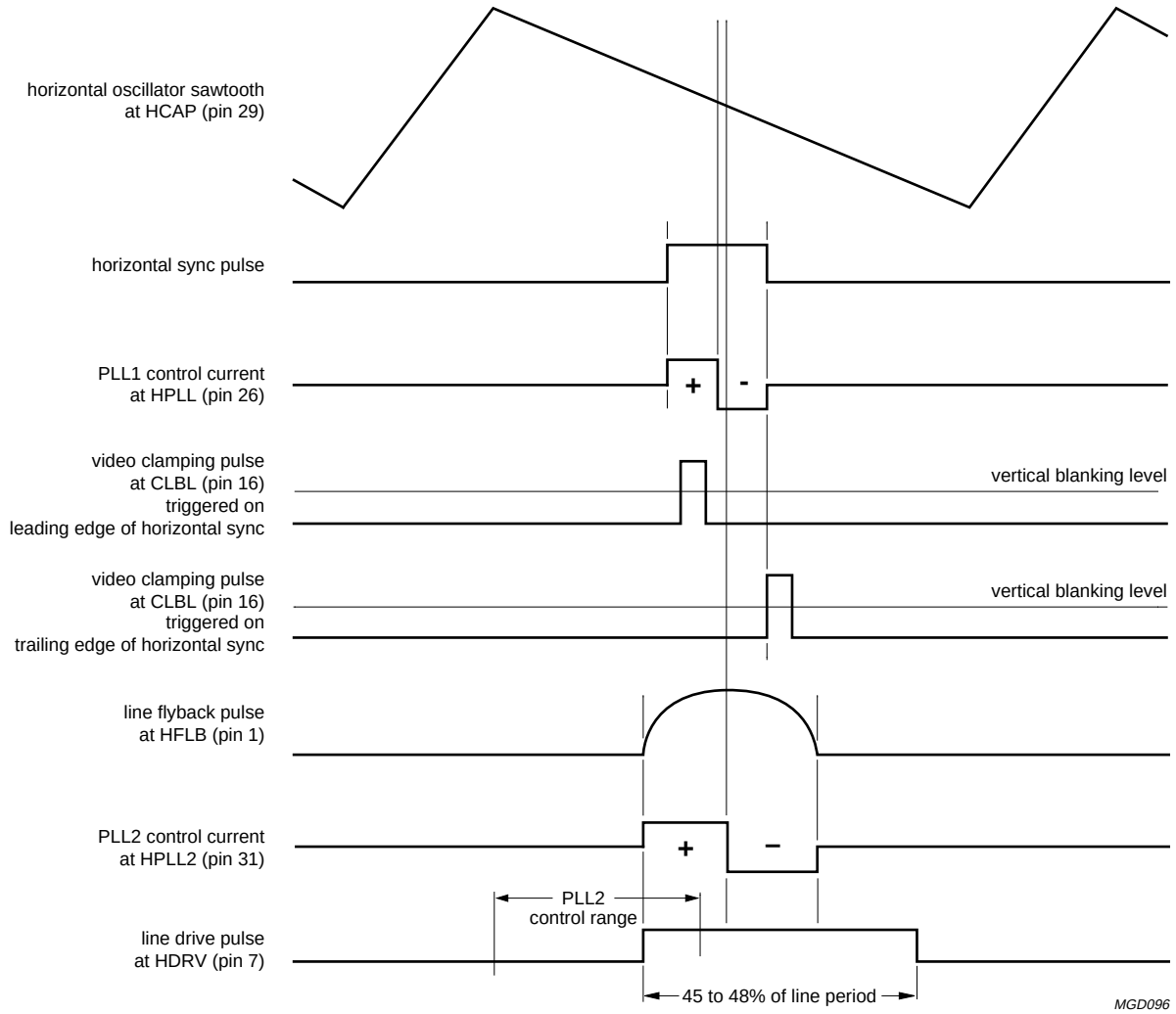


Fig.9 Pulse diagram for horizontal part.

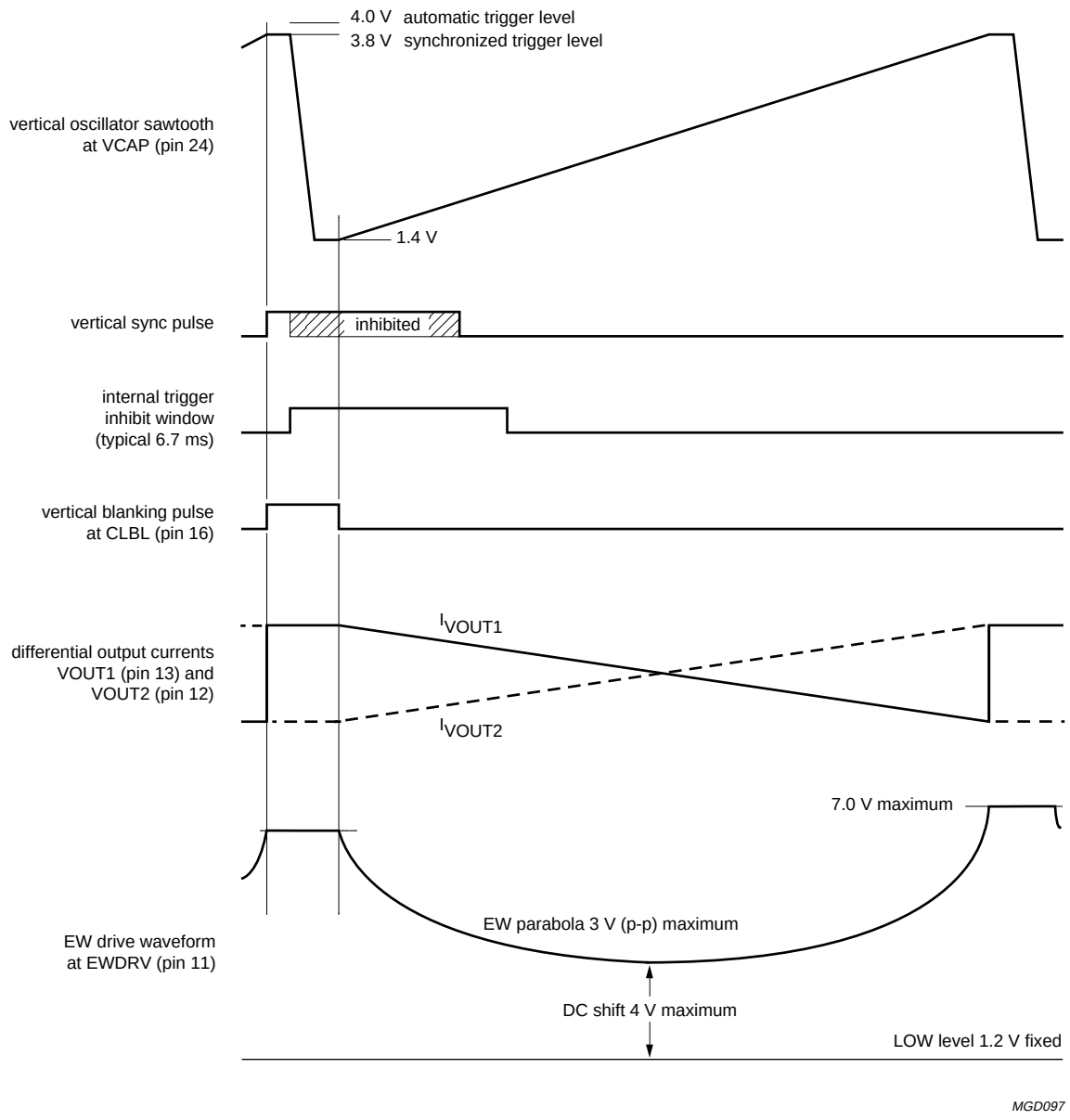
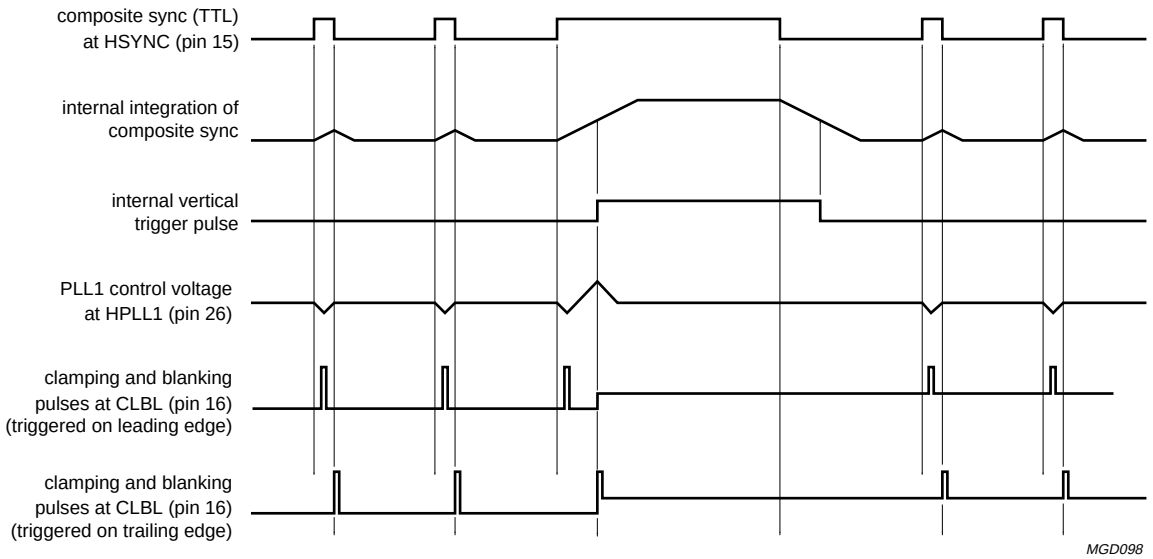
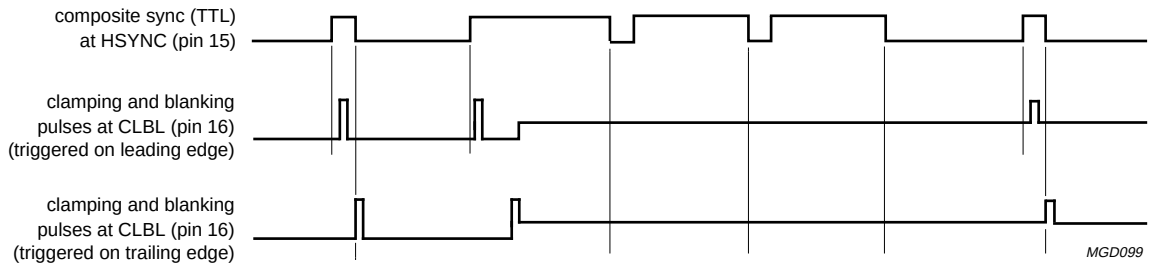


Fig.10 Pulse diagram for vertical part.



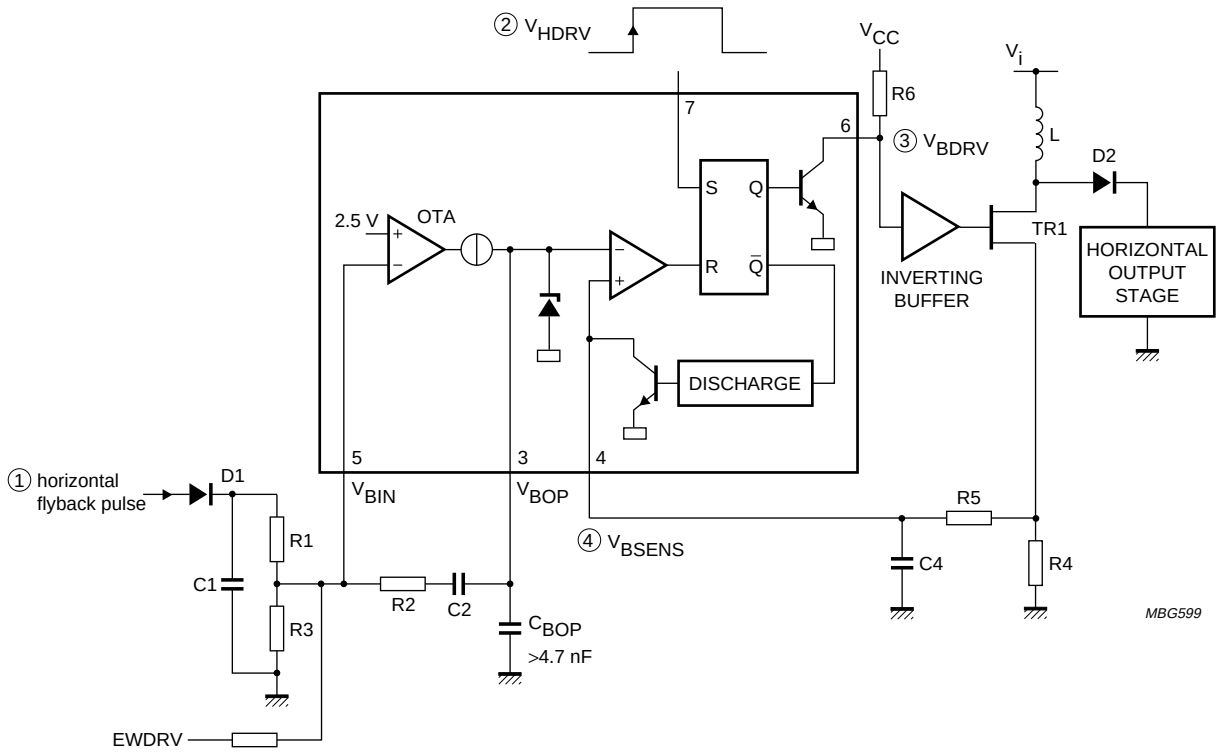
a. Reduced influence of vertical sync on horizontal phase.



b. Generation of video clamping pulses during vertical sync with serration pulses.

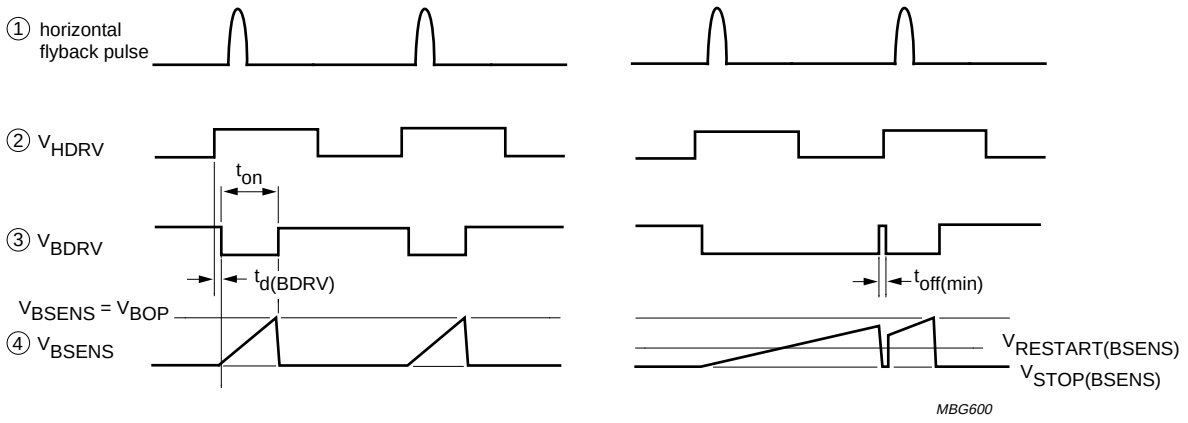
Fig.11 Pulse diagrams for composite sync applications.

APPLICATION INFORMATION



For f < 50 kHz and C2 < 47 nF calculation formulas and behaviour of the OTA are the same as for an OP. An exception is the limited output current at BOP (pin 3). See Chapter “Characteristics”, Row Head “B+ control section (see Figs 12 and 13)”.

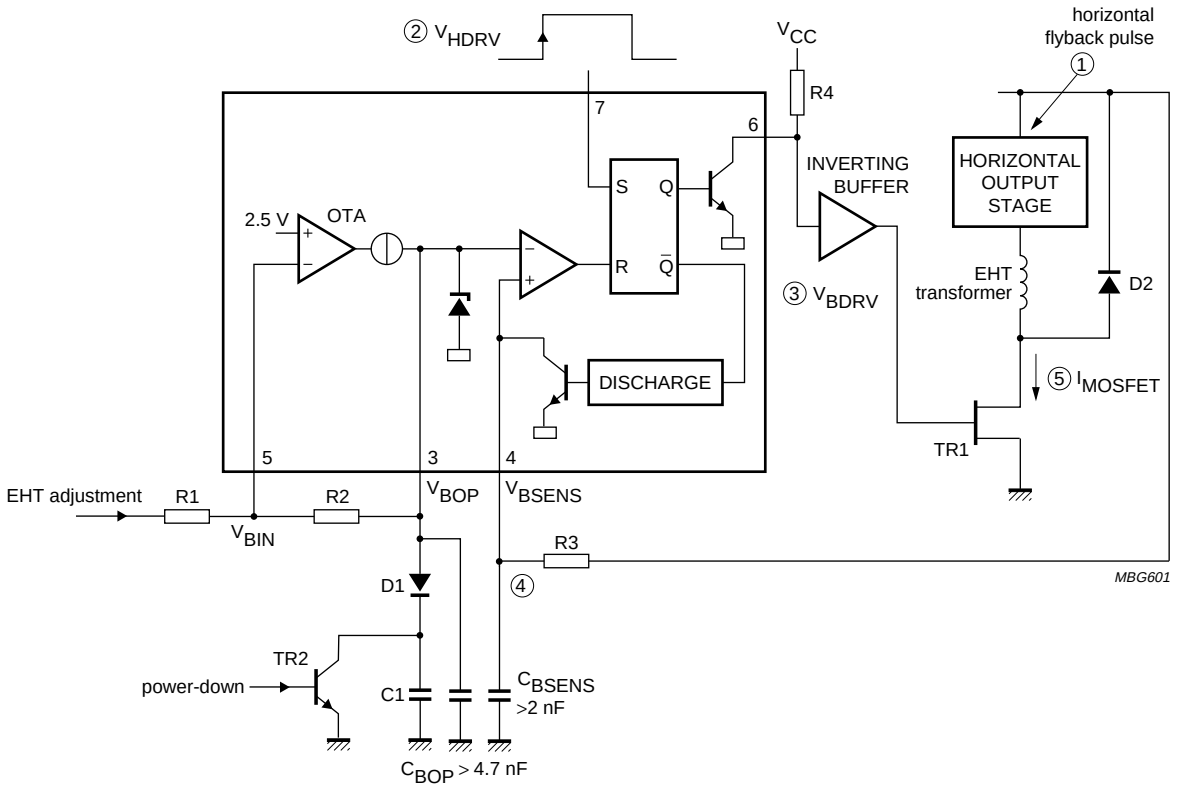
a. Feedback mode application.



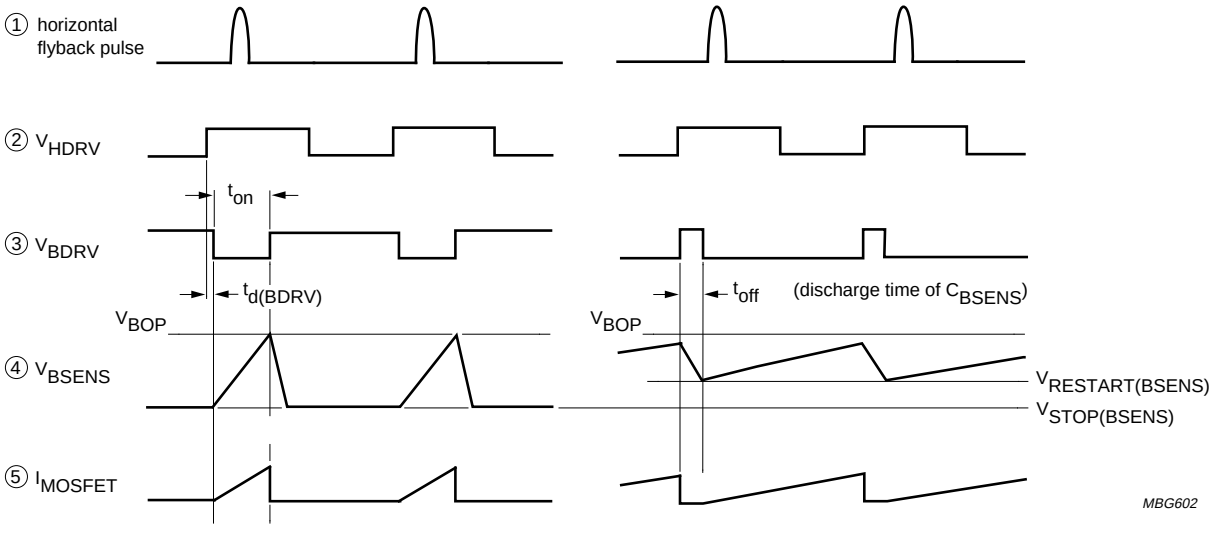
b. Waveforms for normal operation.

c. Waveforms for fault condition.

Fig.12 Application and timing for feedback mode.



a. Forward mode application.

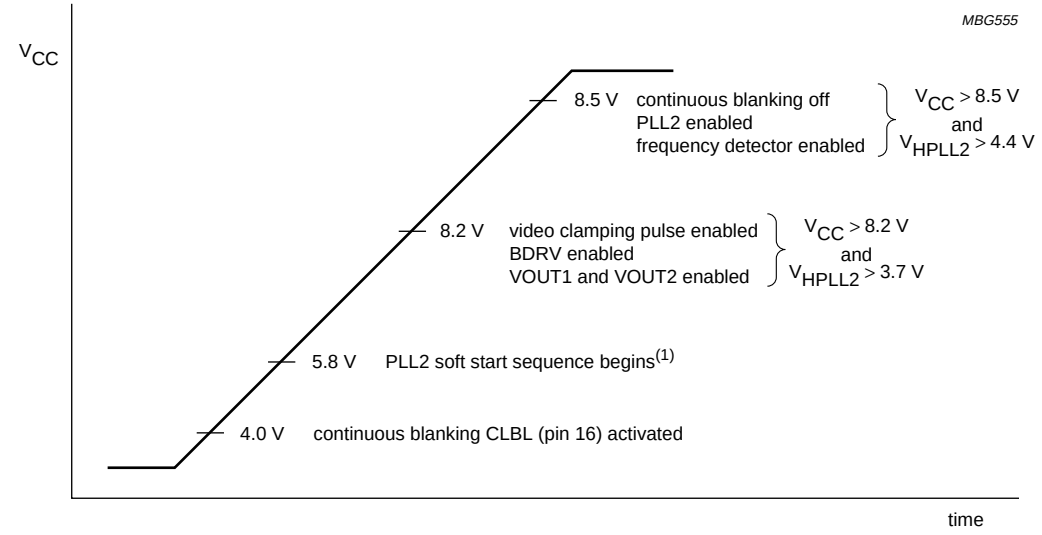


b. Waveforms for normal operation.

c. Waveforms for fault condition.

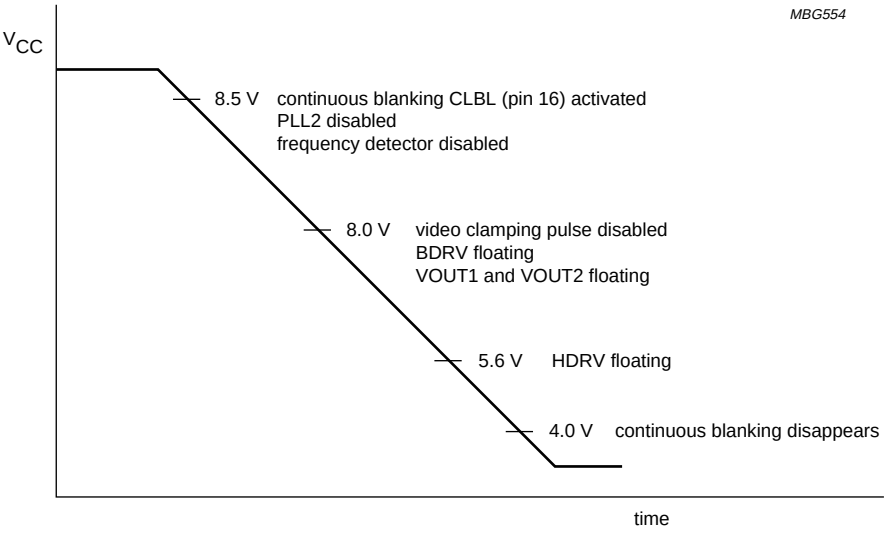
Fig.13 Application and timing for feed forward mode.

Start-up and shut-down sequence



(1) See Fig.15 for PLL2 soft-start.

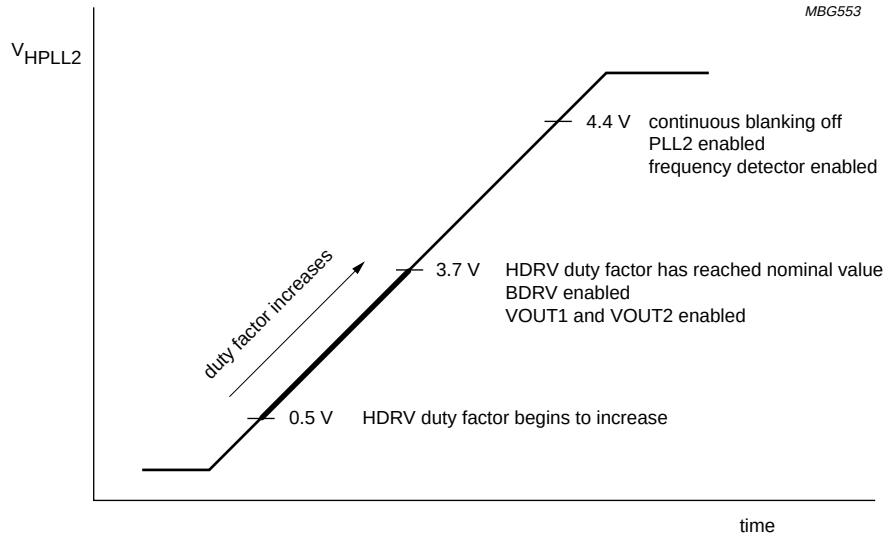
a. Start-up sequence.



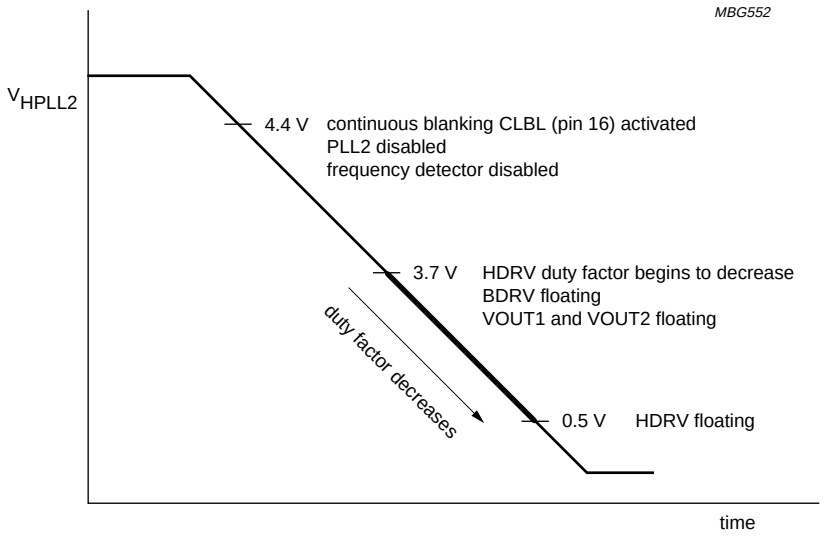
b. Shut-down sequence.

Fig.14 Start-up sequence and shut-down sequence.

PLL2 soft start sequence



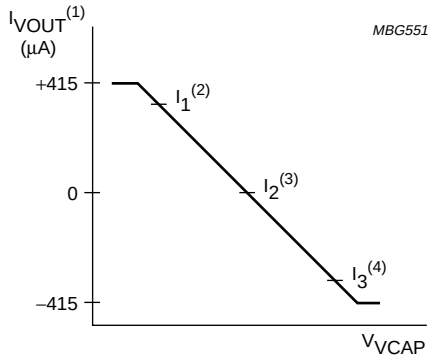
a. PLL2 start-up sequence.



b. PLL2 shut-down sequence.

Fig.15 PLL2 soft start sequence.

Vertical linearity error



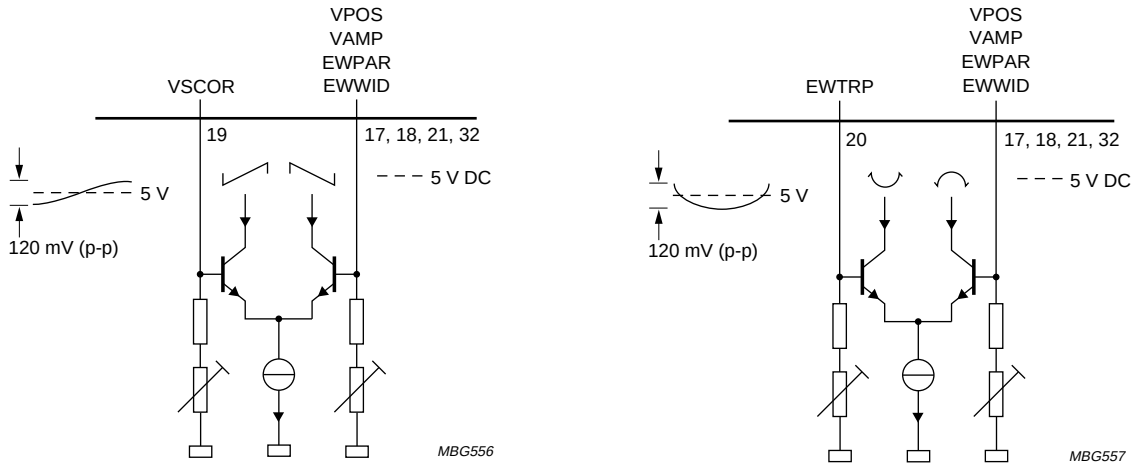
(1) $I_{VOUT} = I_{VOUT1} - I_{VOUT2}$.
(2) $I_1 = I_{VOUT}$ at $V_{VCAP} = 1.9$ V.
(3) $I_2 = I_{VOUT}$ at $V_{VCAP} = 2.6$ V.
(4) $I_3 = I_{VOUT}$ at $V_{VCAP} = 3.3$ V.

Which means: $I_0 = \frac{I_1 - I_3}{2}$

Vertical linearity error = $1 - \max\left(\frac{I_1 - I_2}{I_0} \text{ or } \frac{I_2 - I_3}{I_0}\right)$

Fig.16 Definition of vertical linearity error.

Usage of superimposed waveforms

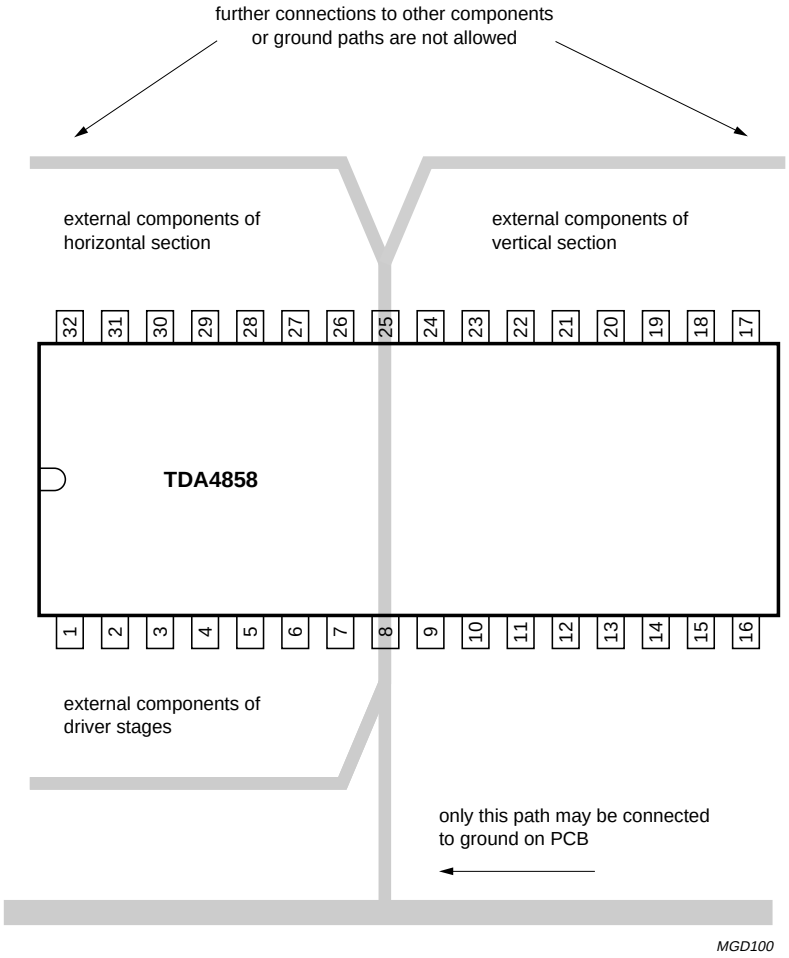


a. VSCOR (pin 19).

b. EWTRP (pin 20).

Fig.17 Superimposed waveforms at pins 19 and 20 with pins 17, 18, 21 or 32.

Printed printed-circuit board layout

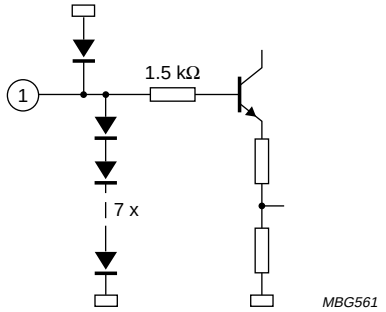
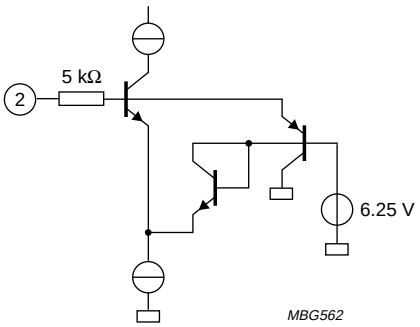
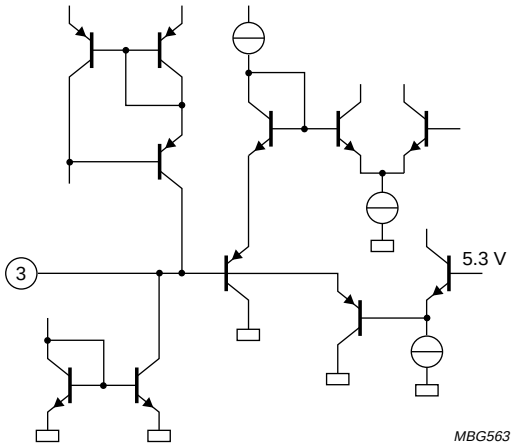


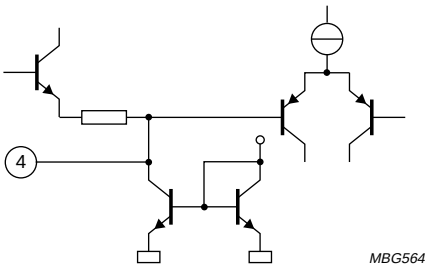
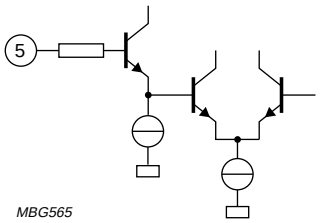
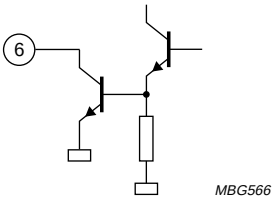
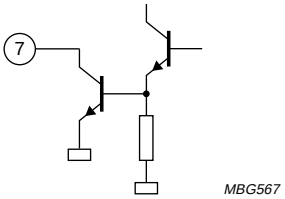
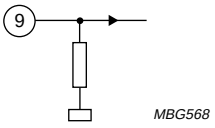
For optimum performance of the TDA4858 the ground paths must be routed as shown. Only one connection to other grounds on the PCB is allowed.

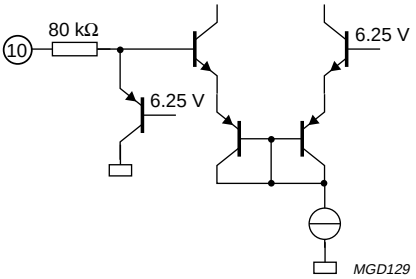
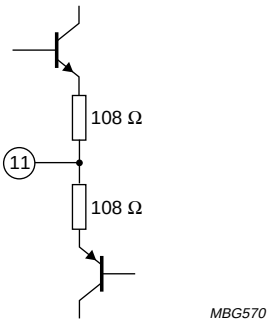
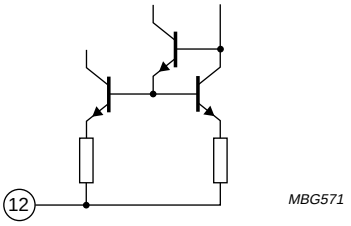
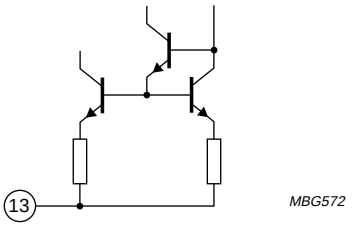
Fig.18 Hints for printed-circuit board (PCB) layout.

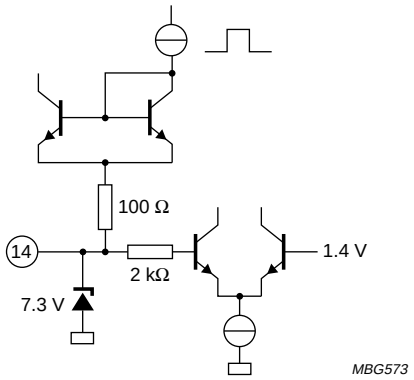
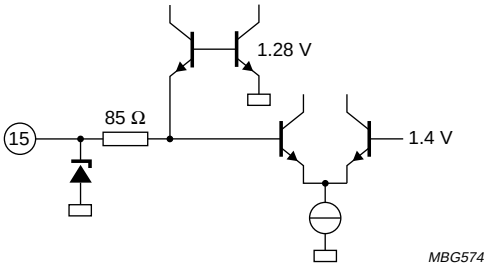
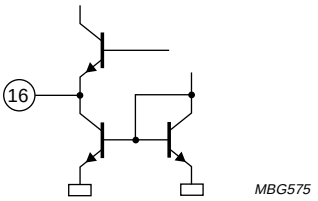
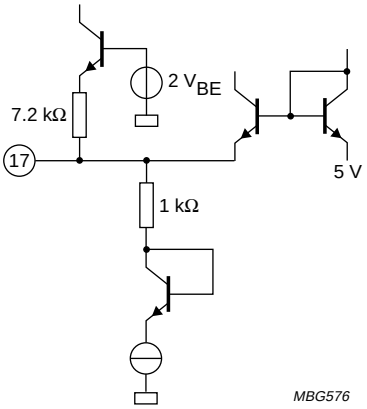
INTERNAL CIRCUITRY

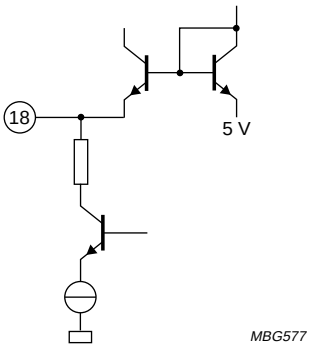
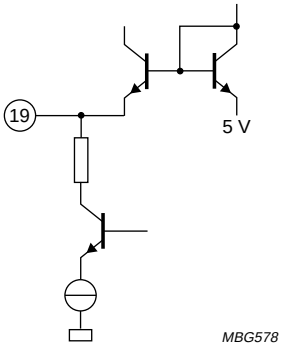
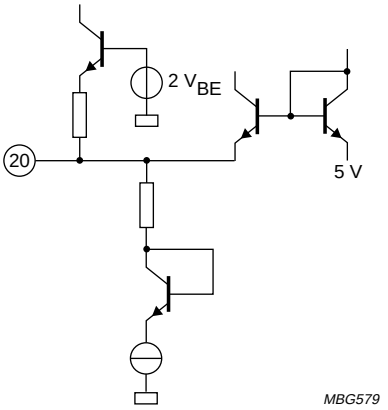
Table 4 Internal circuitry of Fig.1

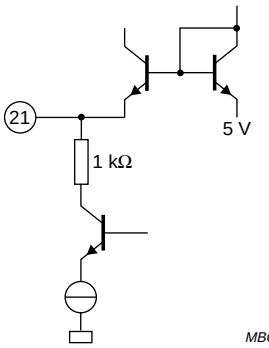
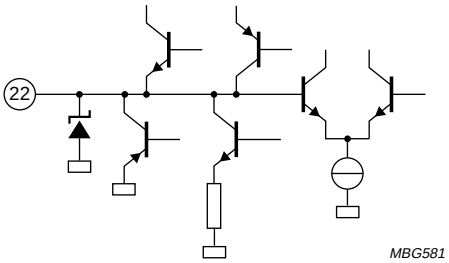
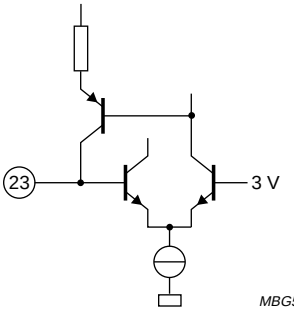
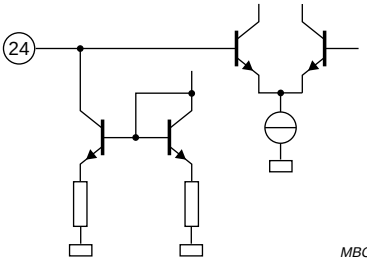
PIN	SYMBOL	INTERNAL CIRCUIT
1	HFLB	
2	XRAY	
3	BOP	

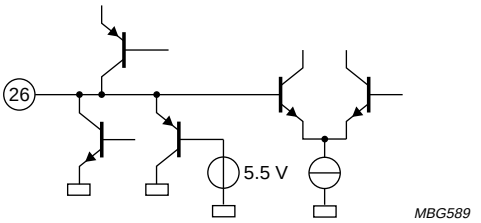
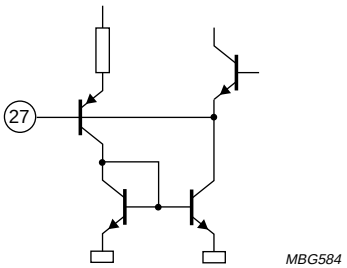
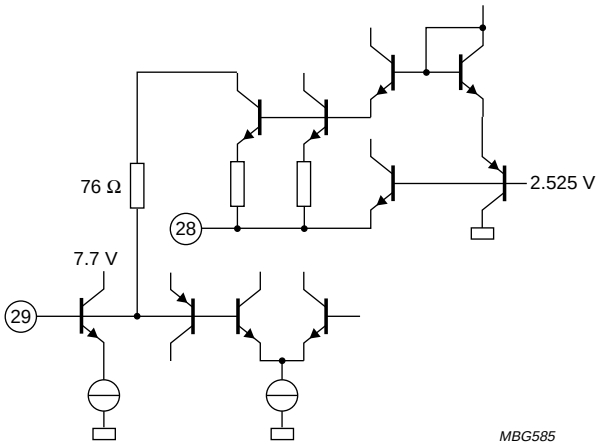
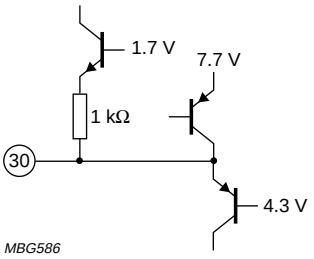
PIN	SYMBOL	INTERNAL CIRCUIT
4	BSENS	
5	BIN	
6	BDRV	
7	HDRV	
8	PGND	power ground, connected to substrate
9	V_{CC}	

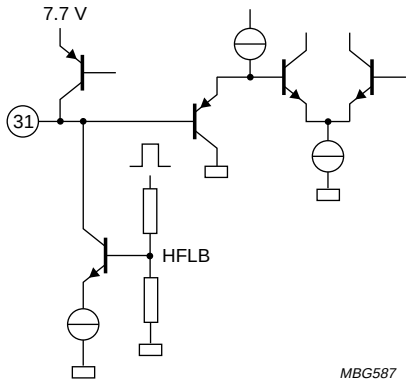
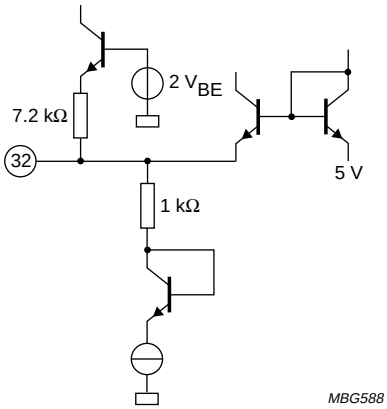
PIN	SYMBOL	INTERNAL CIRCUIT
10	CLSEL	
11	EWDRV	
12	VOUT2	
13	VOUT1	

PIN	SYMBOL	INTERNAL CIRCUIT
14	VSYNC	
15	HSYNC	
16	CLBL	
17	VPOS	

PIN	SYMBOL	INTERNAL CIRCUIT
18	VAMP	
19	VSCOR	
20	EWTRP	

PIN	SYMBOL	INTERNAL CIRCUIT
21	EWPAR	
22	VAGC	
23	VREF	
24	VCAP	
25	SGND	signal ground

PIN	SYMBOL	INTERNAL CIRCUIT
26	HPLL1	
27	HBUF	
28	HREF	
29	HCAP	
30	HPOS	

PIN	SYMBOL	INTERNAL CIRCUIT
31	HPLL2	
32	EWWID	

Electrostatic discharge (ESD) protection

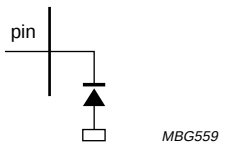


Fig.19 ESD protection for pins 4, 10 to 13 and 16.

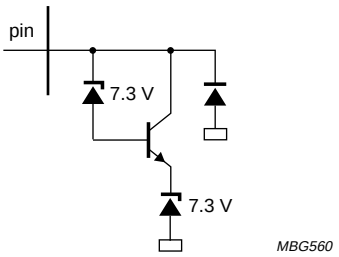
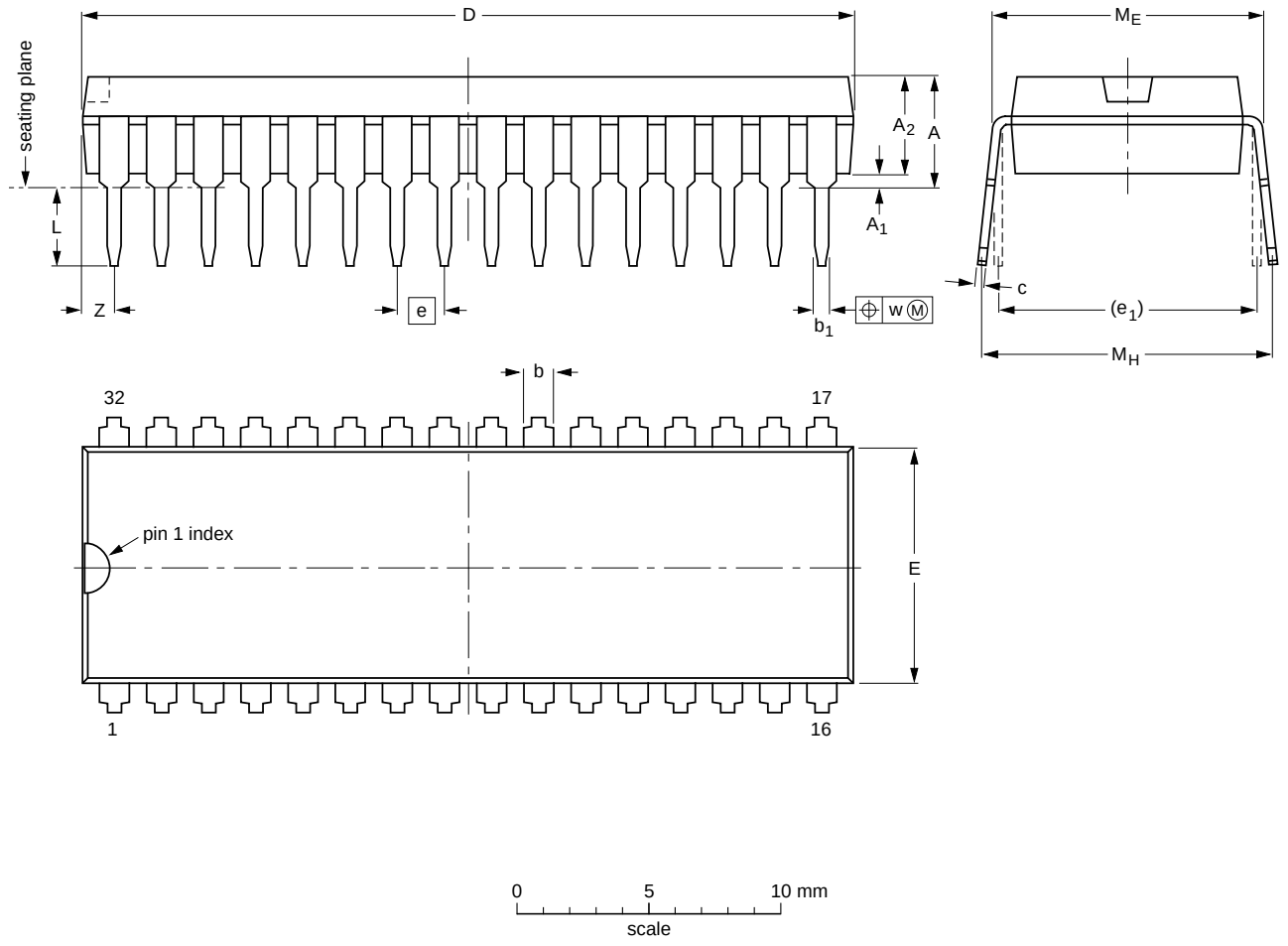


Fig.20 ESD protection for pins 2 to 4, 17 to 24 and 26 to 32.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Printed in The Netherlands 537021/51/01/pp44 Date of release: 1996 Jul 18 Document order number: 9397 750 00974

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